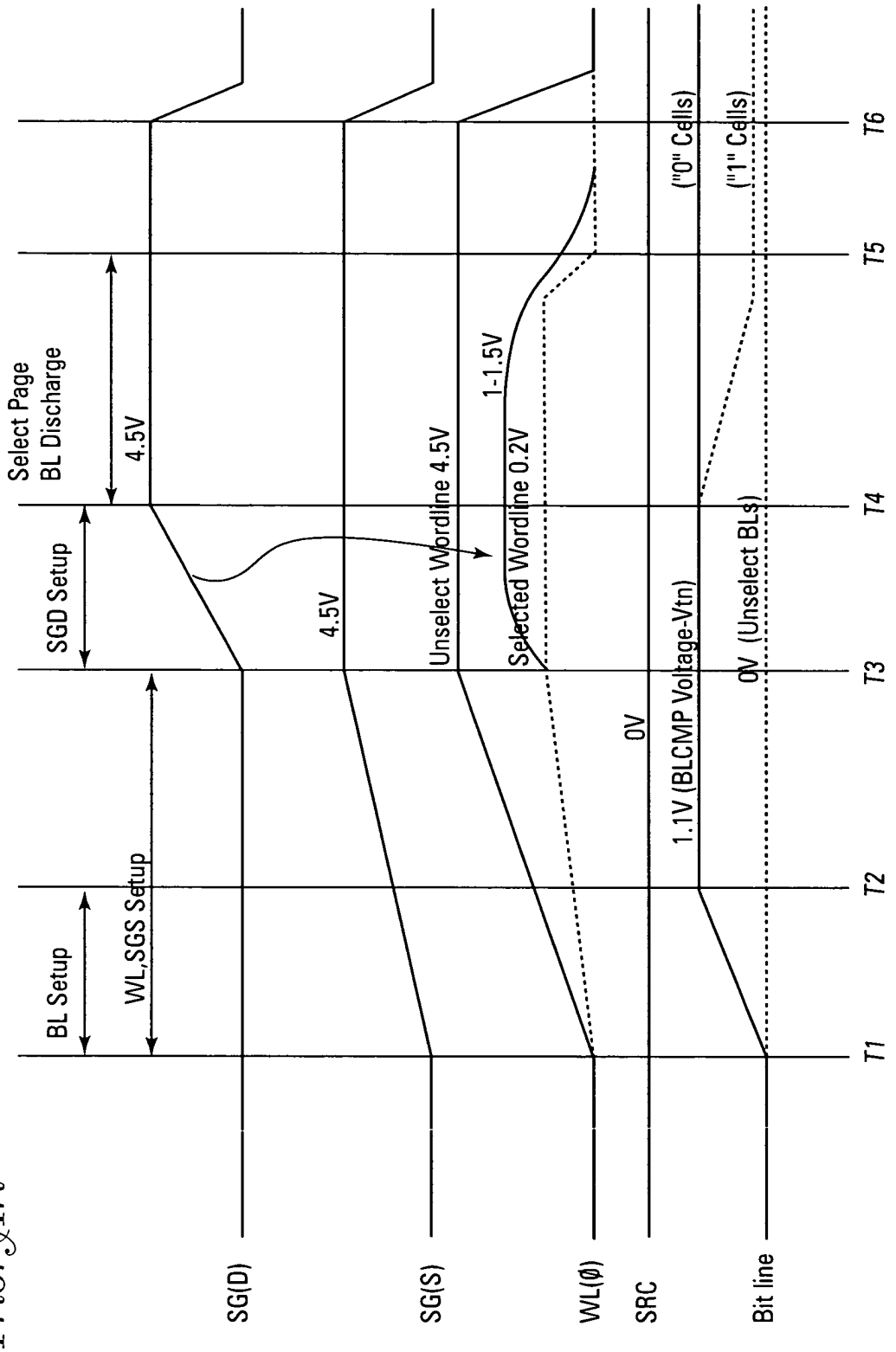

Fig. 1
Prior Art

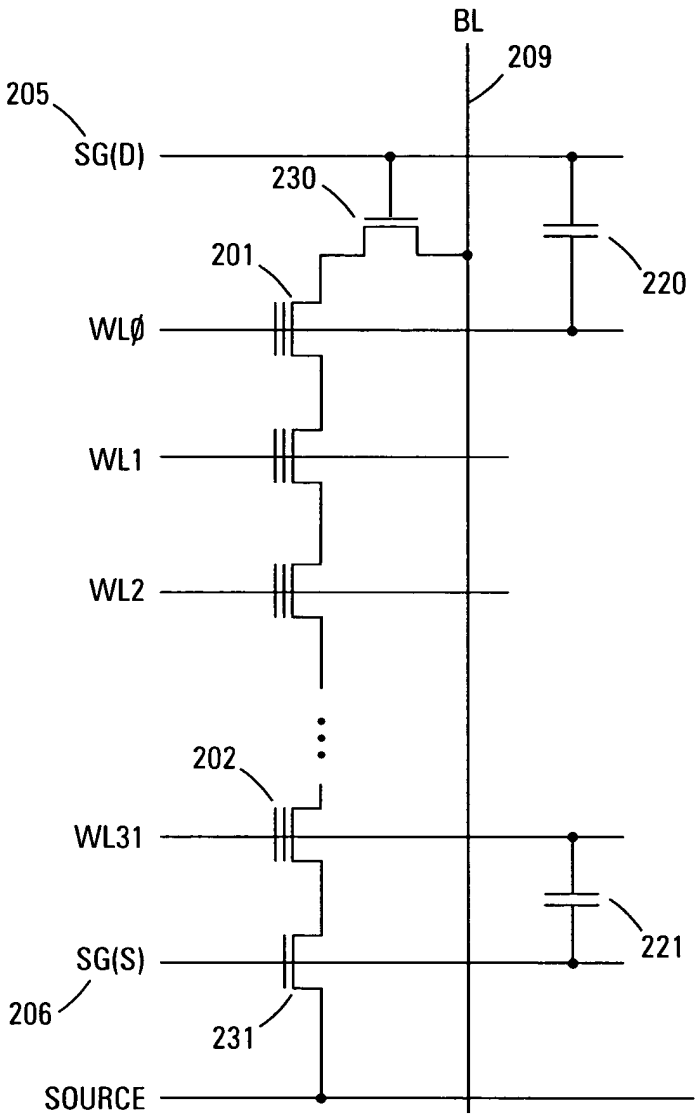
BL
209
205
SG(D)
230
201
220
WLØ
WL1
WL2
202
WL31
221
SG(S)
206
231
SOURCE

Fig. 2

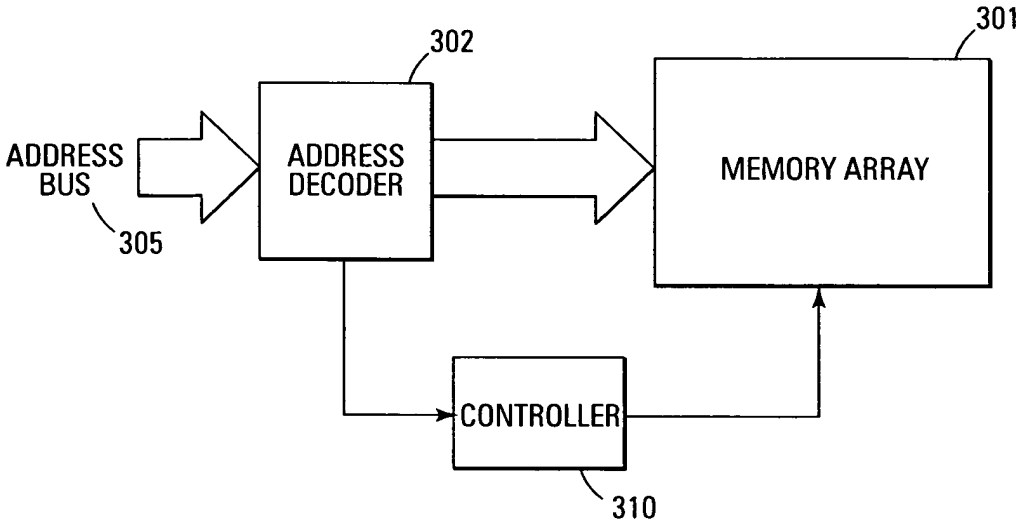
301
302
ADDRESS BUS
305
ADDRESS DECODER
MEMORY ARRAY
CONTROLLER
310

Fig. 3

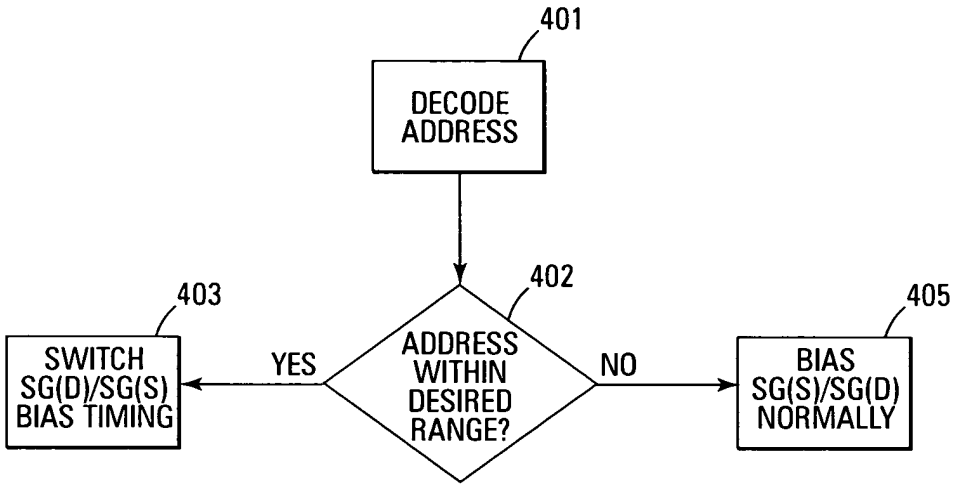
401
DECODE ADDRESS
402
403
405
SWITCH SG(D)/SG(S) BIAS TIMING
YES
ADDRESS WITHIN DESIRED RANGE?
NO
BIAS SG(S)/SG(D) NORMALLY

Fig. 4

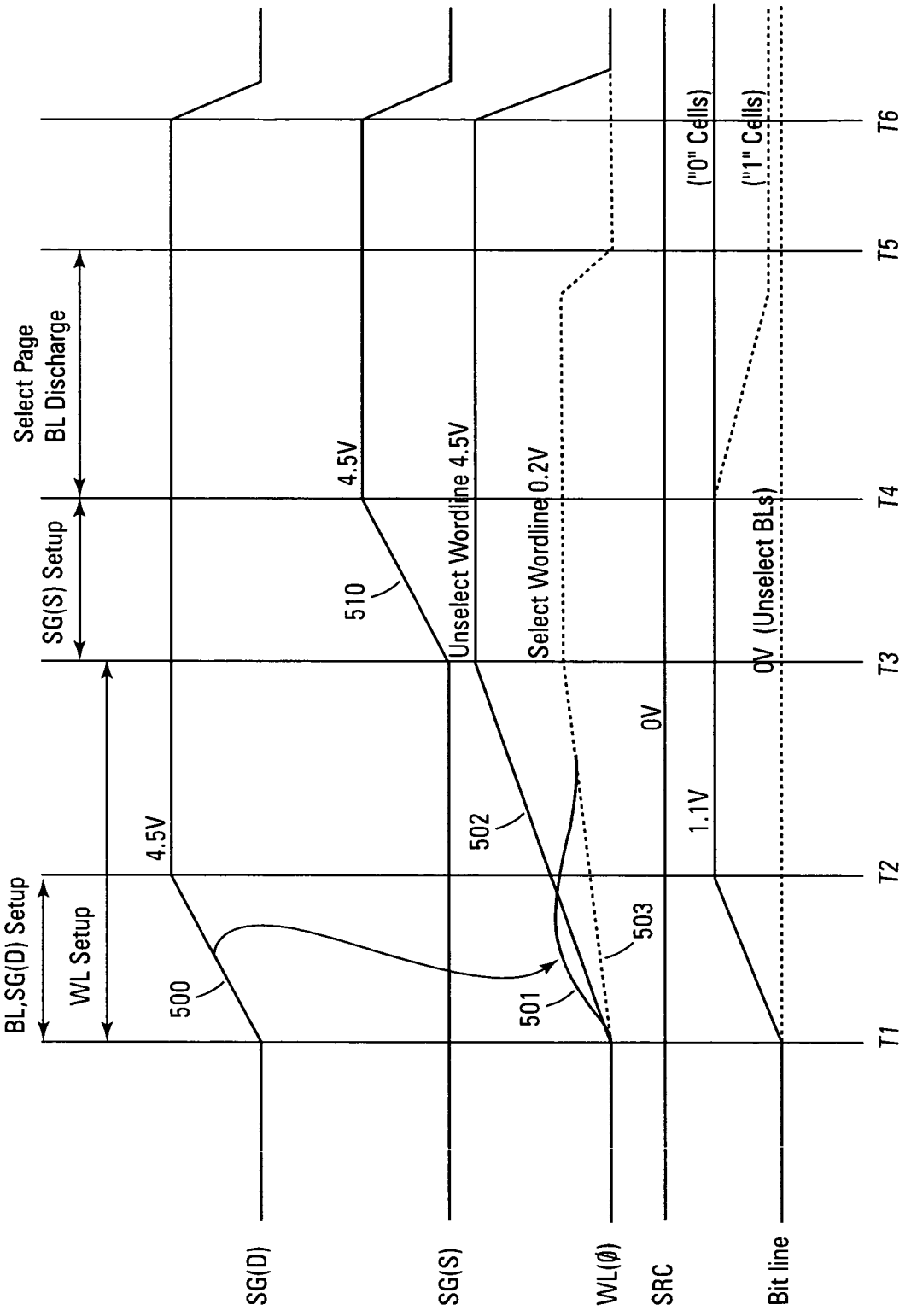
BL,SG(D) Setup
WL Setup
SG(S) Setup
Select Page
BL Discharge
T1
T2
T3
T4
T5
T6
4.5V
4.5V
0V
1.1V
0V (Unselect BLs)
("0" Cells)
("1" Cells)
Unselect Wordline 4.5V
Select Wordline 0.2V
500
501
502
503
510
SG(D)
SG(S)
WL(Ø)
SRC
Bit line

Fig. 5

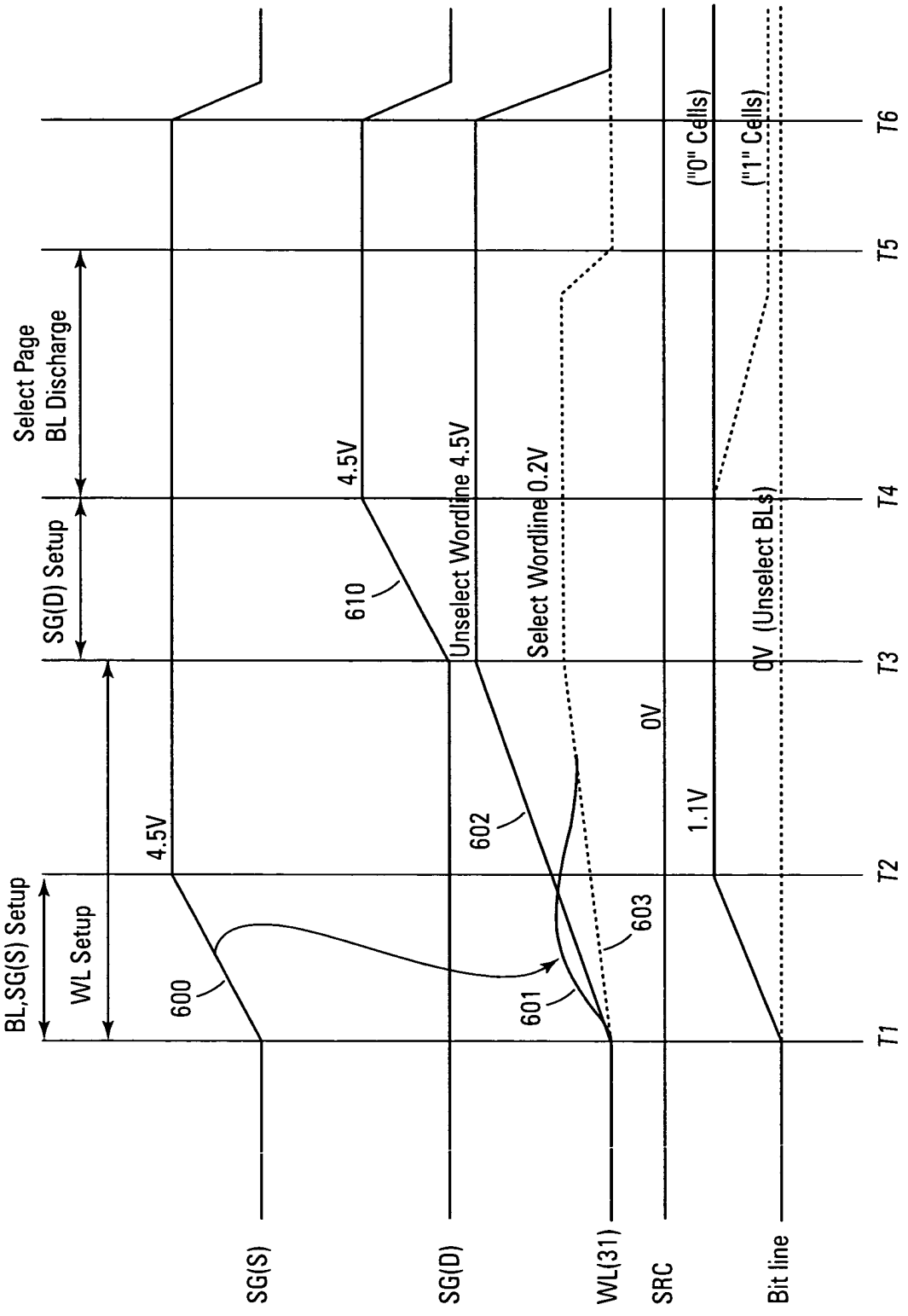
BL,SG(S) Setup
WL Setup
SG(D) Setup
Select Page
BL Discharge
4.5V
4.5V
600
610
602
601
603
Unselect Wordline 4.5V
Select Wordline 0.2V
0V
1.1V
0V (Unselect BLs)
("0" Cells)
("1" Cells)
T1
T2
T3
T4
T5
T6
SG(S)
SG(D)
WL(31)
SRC
Bit line

Fig. 6

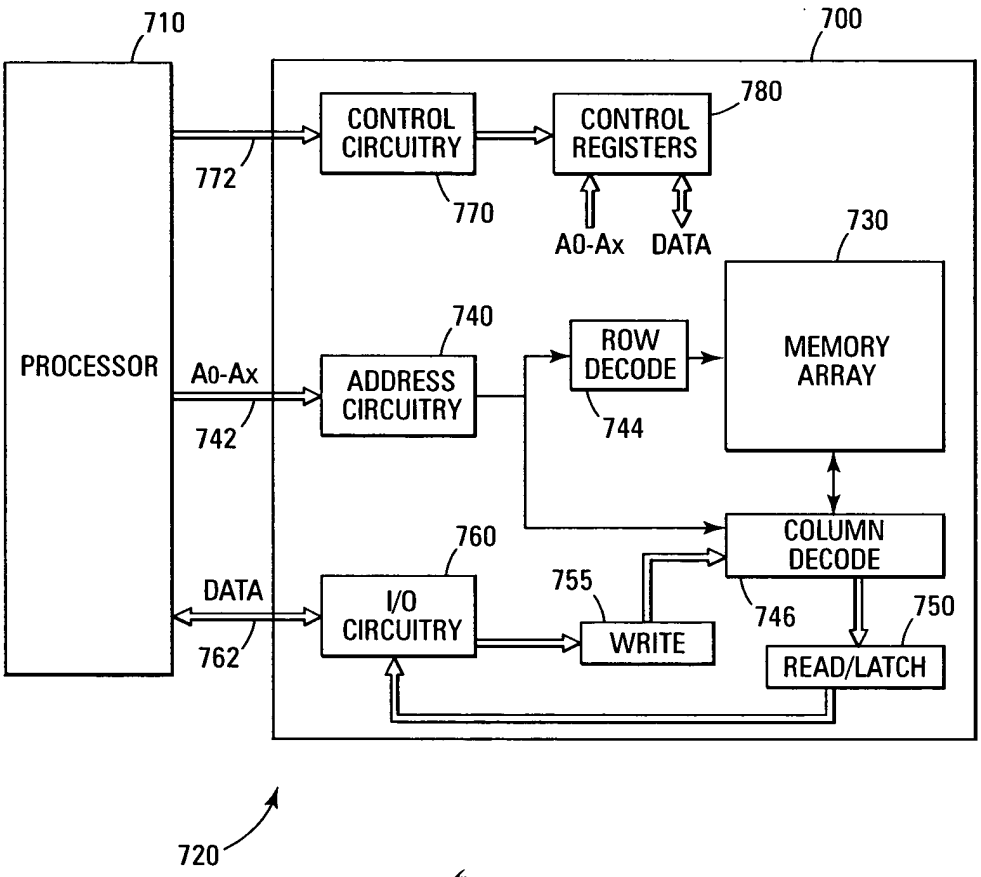
710
700
PROCESSOR
772
CONTROL CIRCUITRY
770
CONTROL REGISTERS
780
A0-Ax
DATA
730
MEMORY ARRAY
740
A0-Ax
742
ADDRESS CIRCUITRY
ROW DECODE
744
COLUMN DECODE
746
760
DATA
762
I/O CIRCUITRY
755
WRITE
750
READ/LATCH
720

Fig. 7